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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,428	03/09/2000	Shunpei Yamazaki	SEL-165	3238

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Cook Alex McFarron Manzo Cummings & Mehler LTD
200 West Adams Street
Suite 2850
Chicago, IL 60606

EXAMINER	
JORGENSEN, LELAND R	
ART UNIT	**PAPER NUMBER**
2675	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/522,428	YAMAZAKI ET AL.
	Examiner	**Art Unit**
	Leland R. Jorgensen	2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 74 and 76 - 153* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 74 and 76 - 153* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 26 April 2005 has been entered.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 5, 10, 11, 29, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al., USPN 5,673,061, in view of Matsueda et al. USPN 6,380,917 B2 and Nakai et al., USPN 6,072,454.

Claim 1

Okada teaches a display device with an active matrix circuit comprising a plurality of pixel TFTs over a substrate. Okada, col. 1, lines 21 – 34; col. 9, lines 34 – 35, 57 – 58; and figure 1. A source driver [data driver 102] and a gate driver [scanning driver 103] drive the active matrix circuit. Okada, col. 9, lines 51 – 60; and figure 1.

Okada teaches that n bit information out of m bit digital video data inputted from an external is used for a voltage gray scale method, V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, and

V_{64}; (m-n) bit information is used for a time ratio gray scale method, $t_0 - t_7$. Okada, col. 11, lines 33 – 37; col. 12, lines 14 - 16; and figure 6. In the example given, m equals 12, n equals 8. Thus, both m and the n are integers equal to or larger than 2. It is inherent that m>n if (m-n) bit information is used for a time ratio gray scale method.

Okada does not teach an D/A converter.

Matsueda teaches a driving circuit and method for an electro-optical device such as a liquid crystal display. The device includes a D/A converter. Matsueda, col. 1, lines 10 – 19. Matsueda teaches that the D/A converter inputs and outputs a high voltage [maximum applied voltage] and low voltage [minimum applied voltage]. Matsueda, col. 4, lines 25 – 45; col. 18, line 28 – col. 19, line 3; and figures 4 & 5. Matsueda also teaches an gray scale of 2^N steps where N is a natural number. Matsueda, col. 2, line 66 – col. 3, line 30. It is inherent that each step of such gray scale would be $(VH - VL)/ 2^N$ where VH is the high voltage and VL is the low voltage input into the D/A converter.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the D/A converter as taught by Matsueda with the display device as taught by Okada to produce a driving circuit that is compatible with digital signal images and has a relatively simple and small-scale circuit. Matsueda, col. 2, lines 58 – 65; col. 26, line 39 – col. 27, line 3.

Neither Okada nor Matsueda teach the first and second TFT.

Nakai teaches an active matrix circuit comprising a plurality of pixels each comprising a first [pixel selecting transistor] and second thin film transistors [n-channel transistor 104 and p-channel transistor 105] and a pixel electrode [liquid crystal layer 106]. The gate electrode of the first thin film transistor is electrically connected to a gate line [scanning line 102]. The gate

electrode of the second thin film transistor is electrically connected to a drain region of the first thin film transistor. The pixel electrode is electrically connected to the drain regions of the second thin film transistors. Nakai, col. 14, lines 29 – 59; and figure 1.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the TFT arrangement as taught by Nakai with the display device as taught by Okada and Matsueda to separate the power TFT from the selection TFT. In the prior art, a single TFT carries too may functions, that is supplying power to the pixel element and selecting the pixel element.

Claim 5

Neither Okada, Matsueda, nor Nakai specifically teach an image gray scale of $(2^m-(2^{m-n}-1))$ patterns.

Okada teaches that patterns that between the specified pair of gray-scale voltages, (2^y-1) intermediate voltages can be obtained. Therefore, the number of obtainable intermediate voltage is $2^x(2^y-1)$, where x plus y equals the number of bits, with x the number of upper bits and y the number of lower bits. Okada, col. 15, line 51 – col. 16, line 33; col. 24, line 50 – 65.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the formula of Okada to obtain the same results as obtained by the formula $(2^m-(2^{m-n}-1))$. But definition, x equals m – n; y equals n. Thus, for m = 6 and n = 3, according to the claim 5 the image gray scale has 57 patterns. According to Okada, the number of intermediate voltages is 56. However, the Okada formula excludes the zero or black value of 000000. If the black value is added to Okada, the image gray scale has 56 plus 1 for 57 patterns. For m = 5 and n = 2,

according to claim 5 the image gray scale has 25 patterns. According to Okada, the number of intermediate voltages is 24 plus the black value of 1 for 25 patterns.

The claim 5 formula can be derived from the Okada formula as follows.

According to Okada, the number of obtainable intermediate voltages is $2^x (2^y - 1)$.

Thus, the number of image gray scale patterns with the black value is $2^x (2^y - 1) + 1$.

Since $x = m - n$ and $y = n$, then

$$2^x (2^y - 1) + 1 = 2^{m-n} (2^n - 1) + 1 = 2^{m-n+n} - 2^{m-n} + 1 = 2^m - 2^{m-n} + 1 = 2^m - (2^{m-n} - 1)$$

Therefore, the claim 5 formula is identical to the Okada formula.

Claims 10 and 29

Okada does not specifically teach that m is 8 and n is 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to create the display device of Okada where m is 8 and n is 2. Okada invites such teaching,

> In the driving circuit in Example 1 described above, a pair of gray-scale voltages are specified from the plurality of gray-scale voltages, based on the upper three bits D_5, D_4, and D_3 of the 6-bit video data D_0, D_1, D_2, D_3, D_4, and D_5. A pair of analog switches corresponding to the specified pair of gray-scale voltages are driven at a duty ratio corresponding to the lower three bits D_2, D_1, and D_0. However, the invention is not limited to this manner.

Okada, col. 15, lines 43 – 50.

> In this example, the number of the oscillating signals t_0 - t_4 has been assumed to be equal to the number of lower bits (i.e., 5) used for specifying the oscillating signal T of the 8-bit video data. However, the invention is not limited to this specific case. For example, some of the oscillating signals t_0 - t_4 can be omitted, because the omitted oscillating signal(s) can be generated by repeatedly using the remaining oscillating signals. Also, the duty ratio of the oscillating signal is not limited to the above-described example.

Okada, col. 21, lines 33 – 41.

Claims 11 and 36

Okada teaches, in an example, that m is 12 and n is 4. Okada, col. 2, line 37 – col. 3, line 20; and figures 22 and 23.

4. Claims 2, 6, 26, 30, 33, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al. in view of Matsueda et al. as applied to claim 1 above, and further in view of Yasunishi, USPN 6,094,243.

Claim 2

Claim 2 describes a display device similar to claim 1 but adds that one frame image comprises 2^{m-n} subframes. Although Okada does not specifically state this formula, it uses the formula to determine the number of required gray-scale voltages. Okada, col. 2, lines 15 – 22. Okada defines the number of video data bits as x + y. Okada, col. 15, lines 51-53; col. 24, lines 50 – 53. As noted in the discussion above, x equals m – n; y equals n; and the m-n is the number of bit information used for the time ratio gray scale method.

Neither Matsueda nor Okada specifically describe m - n subframes having 2^{m-n} levels.

Yasunishi teaches dividing a period T into k subframes with 2^k levels. Yasunishi, col. 8, lines 44 – 67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine k subframes with 2^k levels with the display device of Okada to produce a display device that has each frame image comprising 2^{m-n} subframes. That is, since the claim in light of Okada describes the number of levels as m-n, it follows that dividing the period T into k subframes with 2^k levels could be applied to Okaka to produce 2^{m-n} levels with k = m – n.

"Thus, it is possible to conduct a gray-scale display with 2^k levels by dividing the period T into K subframes." Yasunishi, col. 8, lines 65 – 67. Yasunishi invites such combination by teaching,

> There are provided subframes of a number greater than the bit length of data (i.e., the number of gray-scale bits) which represent the gray-scale levels of input image data. A period and a voltage value are set independently for each subframe, whereby a certain number of gray-scale levels can be effected with a lesser number of subframes as compared to the conventional frame modulation method. Moreover, by setting the period and the voltage value independently for each subframe, it is possible to avoid the reduction in the minimum pulse width which would occur in the conventional pulse width modulation method as the number of gray-scale levels increases. As a result, flickers in the displayed images and the display non-uniformity caused by the waveform distortion can be suppressed.
>
> Furthermore, image data for one frame is processed as binary display data which is set independently for each subframe. Therefore, it is possible to eliminate the complicated large-scale arithmetic circuit for performing square-sum calculation and square-root extraction, and a high-precision liquid crystal driver for outputting the analog voltage amplitude, which are required in the conventional amplitude modulation method.
>
> Furthermore, by setting a voltage amplitude independently for each subframe, it is possible to construct a display device most suitable for the response performance of the liquid crystal panel and the voltage endurance of the liquid crystal driver.
>
> Thus, the invention described herein makes possible the advantages of: (1) providing a liquid crystal display device capable of conducting a gray-scale display while suppressing flickers in the displayed images which would occur in the frame modulation method and suppressing the display non-uniformity which would occur in the pulse width modulation method, without increasing the circuit scale so significantly as in the amplitude modulation method; and (2) providing a method for driving such a liquid crystal display device.

Yasunishi, col. 6, line 52 – col. 7, line 21.

Claim 6

Claim 6 describes a display device similar to claim 2 but adds that an image is displayed by an image gray scale of $(2^m-(2^{m-n}-1))$ patterns. As discussed in the response to claim 5 above, the Okada formula is the same as the $(2^m-(2^{m-n}-1))$ pattern.

Claims 26 and 30

Okada does not specifically teach that m is 8 and n is 2. For the reasons stated in the rejections of claims 10 and 29 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to create the display device of Okada where m is 8 and n is 2.

Claims 33 and 37

Okada teaches, in an example, that m is 12 and n is 4. Okada, col. 2, line 37 – col. 3, line 20; and figures 22 and 23.

5. Claims 3, 27, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al., Matsueda et al., and Nakai, as applied to claim 1 above, and further in view of Yamazaki et al., USPN 6,335,716 B1.

Claim 3

Claim 3 describes a device similar to claim 1 but adds that the active matrix circuit, the drivers, and the converter circuit are formed over a substrate.

Okada specifically teaches that active matrix circuits and drivers are formed over a substrate. Although it is obvious, perhaps inherent, that the converter circuit of Okada would be formed over the same substrate, Okada does not specifically state such.

Yamazaki et al. teaches that all circuits for a display device formed over the same substrate. Yamazaki, col. 3, lines 38 – 50.

It would have been obvious to one of ordinary skill in the art at the time of the invention to form all circuits on the same substrate as taught by Yamazaki including all the circuits taught by Okada et al., Matsueda, and Yasunishi because it is easier and cheaper to manufacture and the display would require less space.

Claim 27

Okada does not specifically teach that m is 8 and n is 2. For the reasons stated in the rejections of claims 10 and 29 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to create the display device of Okada where m is 8 and n is 2.

Claim 34

Okada teaches, in an example, that m is 12 and n is 4. Okada, col. 2, line 37 – col. 3, line 20; and figures 22 and 23.

6. Claims 4, 8, 28, 32, 35, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al., Matsueda et al., and Yasunishi, as applied to claim 2 above, and further in view of Yamazaki et al., USPN 6,335,716 B1.

Claim 4

Claims 4 describes a display device similar to claim 2 but adds that the active matrix circuit, the drivers, and the converter circuit are formed over a substrate.

Okada specifically teaches that active matrix circuits and drivers are formed over a substrate. Although it is obvious, perhaps inherent, that the converter circuit of Okada would be formed over the same substrate, Okada does not specifically state such.

Yamazaki et al. teaches that all circuits for a display device formed over the same substrate. Yamazaki, col. 3, lines 38 – 50.

It would have been obvious to one of ordinary skill in the art at the time of the invention to form all circuits on the same substrate as taught by Yamazaki including all the circuits taught by Okada et al., Matsueda, and Yasunishi because it is easier and cheaper to manufacture and the display would require less space.

Claim 8

Claim 8 describes a display device similar to claim 2 but adds that an image is displayed by an image gray scale of $(2^m-(2^{m-n}-1))$ patterns. As discussed in the response to claim 5 above, the Okada formula is the same as the $(2^m-(2^{m-n}-1))$ pattern.

Claims 28 and 32

Okada does not specifically teach that m is 8 and n is 2. For the reasons stated in the rejections of claims 10 and 29 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to create the display device of Okada where m is 8 and n is 2.

Claims 35, and 39

Okada teaches, in an example, that m is 12 and n is 4. Okada, col. 2, line 37 – col. 3, line 20; and figures 22 and 23.

7. Claims 7, 31, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al. in view of Matsueda et al. and Nakai et al. as applied to claim 1 above, and further in view of Yamazaki et al.

Claim 7

Claim 7 describes a display device similar to claim 1 but adds that all circuits are formed on the same substrate and that an image is displayed by an image gray scale of $(2^{m}-(2^{m-n}-1))$ patterns. As discussed in the response to claim 5 above, the Okada formula is the same as the $(2^{m}-(2^{m-n}-1))$ pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to form all circuits on the same substrate as taught by Yamazaki including all the circuits taught by Okada et al., Matsueda, and Nakai because it is easier and cheaper to manufacture and the display would require less space.

Claim 31

Okada does not specifically teach that m is 8 and n is 2. For the reasons stated in the rejections of claims 10 and 29 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to create the display device of Okada where m is 8 and n is 2.

Claims 38

Okada teaches, in an example, that m is 12 and n is 4. Okada, col. 2, line 37 – col. 3, line 20; and figures 22 and 23.

8. Claims 12 – 17, 40 – 74, 76 - 82, and 89 - 152 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., or Holmes et al., USPN 3,792,919, or Kimura, USPN

5,610,741, or Munyan, USPN 5,761,485, or Stambolic et al., USPN 5,893,798, or Kleinschmidt et al., USPN 6,085,112, or Sato, USPN 6,167,208, or Yun et al., USPN 5,835,139, in view of Okada et al., Nakai et al, and Matsueda et al. as applied to claim 1 or 5 above, or of Okada et al., Matsueda et al., and Yasunishi as applied to claim 2 or 6 above, or of Okada et al., Matsueda et al., Yasunishi, and Yamazaki as applied to claim 4 or claim 8 above, or of Okada et al., Matsueda, Nakai et al, and Yamazaki as applied to claim 3 and 7 above.

Claims 12 – 17, 40 – 74, 76 - 82, and 89 - 152

As to claims 12, 40 - 46, Yamazaki teaches a rear projector comprising three display devices Yamazaki, col. 16, lines 1 – 25; and figure 11. As to claims 13, 47 – 53, Yamazaki teaches a front projector comprising three display devices. Yamazaki, col. 15, lines 32 – 56; and figure 10. As to claims 14, 54 - 60, Holmes teaches a single plate type rear projector. Holmes, col. 8, lines 48 – 58. As to claims 15, 61 - 67, Yamazaki teaches a goggle type display comprising two display devices. Yamazaki, col. 26, lines 38 – 40; and figure 22D. As to claims 16, 68 - 74, Kimura teaches a display for portable information terminal. Kimura, col. 1, lines 11 – 16. As to claims 17, 76 - 82, Yun et al., teaches a notebook type personal computer. Yun, col. 1, lines 49 – 52; and figure 9. As to claims 89 - 96, Yamazaki teaches a mobile telephone. Yamazaki, col. 26, lines 26 – 29. As to claims 97 - 104, Yamazaki teaches a video camera. Yamazaki, col. 26, lines 29 – 33; and figure 22B. As to claims 105 - 112, Yamazaki teaches a mobile computer. Yamazaki, col. 26, lines 34 – 37; and figure 22C. As to claims 113 - 120, Munyan teaches a portable electric book. Munyan, col. 1, lines 56 – 57. As to claims 121 - 128, Kimura teaches a personal computer. Kimura, col. 1, lines 11 – 16. As to claims 129 - 136, Stambolic et al. teaches a electronic game device. Stambolic, col. 1, lines 9 – 10. As to claims

137 - 144, Kleinschmidt teaches an image reproduction device. Kleinschmidt, col. 5, lines 58 – 61. As to claims 145 - 152, Sato teaches a digital camera. Sato, col. 1, lines 7 – 10.

None of these patents specifically teach the display device of Okada.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the display device of Okada for these generally small appliances. Okada teaches,

> Accordingly, it is unnecessary to provide an additional driving circuit depending on the cases where the driving circuit directly outputs one of the plurality of gray-scale voltages and where the driving circuit alternately outputs the specified pair of gray-scale voltages. As a result, it is possible to simplify the configuration of the driving circuit, and the size of the driving circuit can be minimized.
>
> Thus, the invention described herein makes possible the advantage of providing a driving circuit for a display apparatus, which has a simplified and small construction, and which can display an image with multiple gray scales in accordance with multi-bit video data.

Okada, col. 7, line 59 – col. 8, line 3.

9. Claims 9 and 19 - 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al., Matsueda et al., and Nakai et al., as applied to claim 1 or 5 above, or of Okada et al., Matsueda et al., and Yasunishi as applied to claim 2 or 6 above, or of Okada et al., Matsueda et al., Yasunishi, and Yamazaki as applied to claim 4 or claim 8 above, or of Okada et al., Matsueda et al., Nakai et al., and Yamazaki as applied to claim 3 or 7 above, and further in view of Wu et al., USPN 6,245,256 B1.

Claims 9 and 19 - 25

Okada does not teach thresholdless antiferroelectric mixed liquid crystal.

Wu teaches thresholdless antiferroelectric mixed liquid crystal indicating electro-optical characteristic of V-shape. Wu, col. 3, lines 2 –25; and figure 12.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the antiferroelectric mixed liquid crystal of Wu with the display device of Okada. Wu teaches,

> According to Inui's report, when the mixing ratio of I:II:III=40:40:20, no E_{th} value is found, and its field-induced antiferroelectric to ferroelectric switching shows a V-shaped switching (see FIG. 12). Inui give the name of "Thresholdless antiferroelectric liquid crystals; TLAFLCs" to this antiferroelectric liquid crystal mixture. These thresholdless antiferroelectric liquid crystals have the following properties:
>
> (1) Great tilt angle (>35.degree.);
>
> (2) Low driving voltage (<2V/Tm^{-1});
>
> (3) Ideal gray scale;
>
> (4) Fast antiferroelectric to ferroelectric switching time (<50.mu.s);
>
> (5) High contrast value (>100); and
>
> (6) Broad viewing angle (>60.degree.).
>
> The aforesaid properties eliminate the gray scale problem occurred during the fabrication of a passive matrix addressing (PM) surface stable ferroelectric liquid crystal display, and also improve the drawback of being difficult to obtain a high contrast ratio commonly existed in regular active matrix (AM) or thin film transistor (TFT) addressing type deformed-helix ferroelectric liquid crystal displays and passive matrix addressing type antiferroelectric liquid crystal displays.

Wu, col. 3, lines 2 –25.

10. Claims 18, 84 – 88, and 153 are rejected under 35 U.S.C. 103(a) as being unpatentable Okada et al., Matsueda et al., and Nakai as applied to claim 1 or 5 above, or of Okada et al.,

Matsueda et al., and Yasunishi as applied to claim 2 or 6 above, or of Okada et al., Matsueda et al., Yasunishi, and Yamazaki as applied to claim 4 or claim 8 above, or of Okada et al., Matsueda et al., Nakai et al, and Yamazaki as applied to claim 3 or 7 above, and further in view of Bhargava, USPN 5,455,489.

Claims 18, 83 – 88, and 153

Okada does not teach an EL display.

Bhargava teaches an EL display. Bhargava, col. 9, lines 46 – 64.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the EL display of Bhargava with the display device of Okada. Bhargava teaches,

> Today, EL displays offer unique properties such as flat-slim and high contrast but suffer from (1) poor efficiency, (2) limited color availability and control, (3) lack of gray scale, and (4) expensive drives for high voltage operation.
>
> As will be clear from the foregoing exposition, an EL display whose phosphor layer comprises a DNC particle layer will exhibit higher efficiency, improved gray scale, and due again to its tiny sized particles will operate at low voltages.

Bhargava, col. 9, line 60 – col. 10, line 2. This is especially true in light of Okada's invitation.

> Thus, the invention described herein makes possible the advantage of providing a driving circuit for a display apparatus, which has a simplified and small construction, and which can display an image with multiple gray scales in accordance with multi-bit video data.

Okada, col. 7, line 66 – col. 8, line 3.

Response to Arguments

11. Applicant's arguments with respect to independent claims 1, 3, 5, and 7 and those claims dependant on claims 1, 3, 5, and 7 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 26 April 2005 have been fully considered but they are not persuasive.

As to claims 2, 4, 6, and 8, applicant argued that the claims include one frame period comprises 2^{m-n} subframe periods while Yasunishi teaches dividing a period T into k subframes with 2^k levels. Yasunishi, col. 8, lines 44 – 67. It would have been obvious, however, to one of ordinary skill in the art at the time of the invention to combine k subframes with 2^k levels with the display device of Okada to produce a display device that has each frame image comprising 2^{m-n} subframes. That is, since the claim in light of Okada describes the number of levels as m-n, it follows that dividing the period T into k subframes with 2^k levels could be applied to Okaka to produce 2^{m-n} levels with k = m – n. "Thus, it is possible to conduct a gray-scale display with 2^k levels by dividing the period T into K subframes." Yasunishi, col. 8, lines 65 – 67.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Luo et al., USPN 4,042,854 teaches a first TFT [switching transistor T_1] and second [power transistor T_2] TFT. The drain of the first TFT is connected to the gate of the second

TFT. Imai, USPN 6,369,758 B1 teaches a first TFT [FET 101] and second [FET 102] TFT. The drain of the first TFT is connected to the gate of the second TFT.

Yamazaki et al, USPN 5,349,366, teaches a first TFT [Tr1 and a second TFT [Tr2]. Yamazaki notes,

> A problem in a conventional TFTLCD is, to the knowledge of the present inventors, that a single TFT carries over too many functions. More specifically, a TFT in a conventional TFTLCD has two functions; one is to select a particular pixel, and the other is to supply the electric power to the pixel electrode. It is therefore impossible to further expect on the TFT to achieve two objects at the same time, i.e., rendering the display a memory function and switching the polarity of the high voltage state periodically.

Yamazaki, col. 7, lines 18 – 27.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland R. Jorgensen whose telephone number is 571-272-7768. The examiner can normally be reached on Monday through Friday, 10:00 am through 6:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

On July 15, 2005, the Central FAX Number will change to 571-273-8300. This new Central FAX Number is the result of relocating the Central FAX server to the Office's Alexandria, Virginia campus.

Most facsimile-transmitted patent application related correspondence is required to be sent to the Central FAX Number. To give customers time to adjust to the new Central FAX Number, faxes sent to the old number (703-872-9306) will be routed to the new number until

September 15, 2005. After September 15, 2005, the old number will no longer be in service and 571-273-8300 will be the only facsimile number recognized for "centralized delivery".

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

lrj

Kent Chang

KENT CHANG
PRIMARY EXAMINER